SAYFU MULTILAYER CIRCUITS CO., LIMITED

Design For Manufacturability

Content

Content

Section A : Introduction

This document provide Design For Manufactrability (DFM) to let PCB designer to know the rule of PCB fabrication, & to ensure that the circuit function will meet the requirement, so as to :

1. Raise the fabrication efficiency.
2. Shorten the lead time.
3. Increase the utilization of manufacturing.
4. Reduce the material & labor cost.
5. Minimize the environmental impact.

To achieve these benefits, this document will enable the PCB designer to understand the design rule of PCB fabrication in the following fields :

1. Raw Material
2. Circuit Design
3. Hole
4. Solder Mask
5. Outline
6. Surface Treatment

Section B : Raw Material

Raw material is the most impact of pcb cost, it will take about 20~30% for normal FR4 board cost, and for special material maybe up to 50%. The raw material cost is affected by material type, production panel utilization & stack up.

This section introduces normal raw material type, the production panel design & stack up design.

Section B-1 : Material Base Property

Laminate

FR4 is the E-glass reinforced bifunctional or tetrafuctional expoxy resin base laminate. It is the common material to be used. Besides FR4, some other materials such as Halogen Free, BT, Getek & Rogers & Metal core are also to be used for some time.

Normally, we control the dielectric thickness by the tolerance of class B per IPC-4101A. Detail can be found from the chart in the right.

Nominal Thickness of Laminate (mil)	Class A/K (mil)	Class B/L (mil)	Class C/M (mil)
0.9-4.7	+/−0. 984	+/−0. 709	+/−0. 512
4.7-6.5	+/−1. 5	+/−0. 984	+/−0. 709
6.5-11.8	+/−1. 97	+/−1. 5	+/−0. 984
11.8-19.6	+/−2. 52	+/−1. 97	+/−1. 5
19.7-30.9	+/−2. 95	+/−2. 52	+/−1. 97
30.9-40.9	+/−6. 5	+/−3. 94	+/−2. 95
40.9-65.94	+/−7. 48	+/−5. 12	+/−2. 95
65.94-100.94	+/−9. 06	+/−7. 09	+/−3. 94
100.94-140.91	+/−11. 8	+/−9. 06	+/−5. 12
140.94-250.0	+/−22. 0	+/−11. 8	+/−5. 91

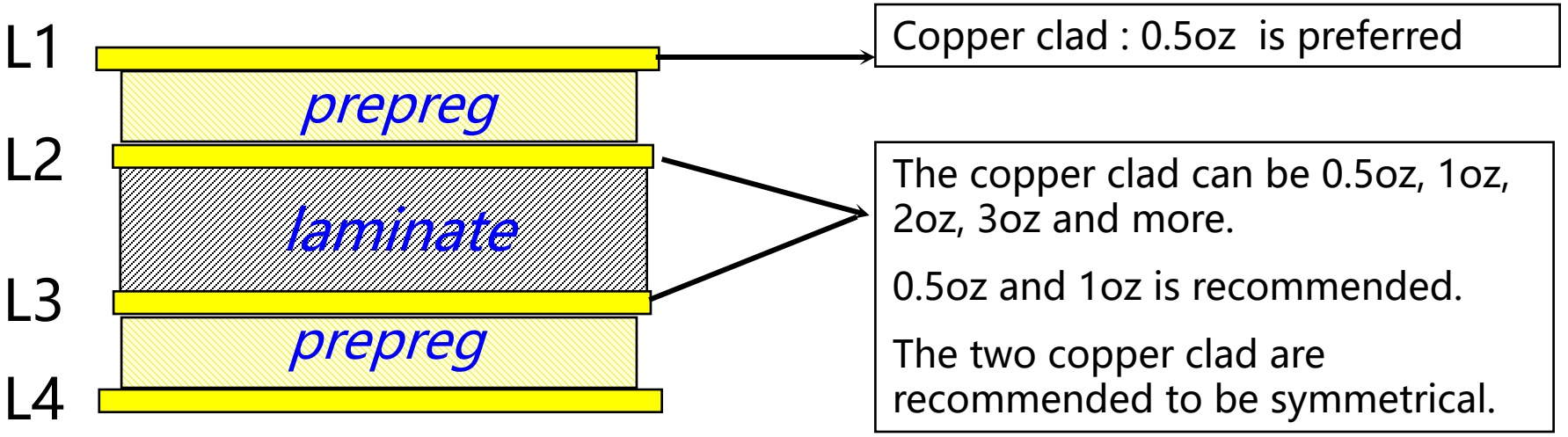
Note : We can control the dielectric thickness by class C, but the cost will be very high.

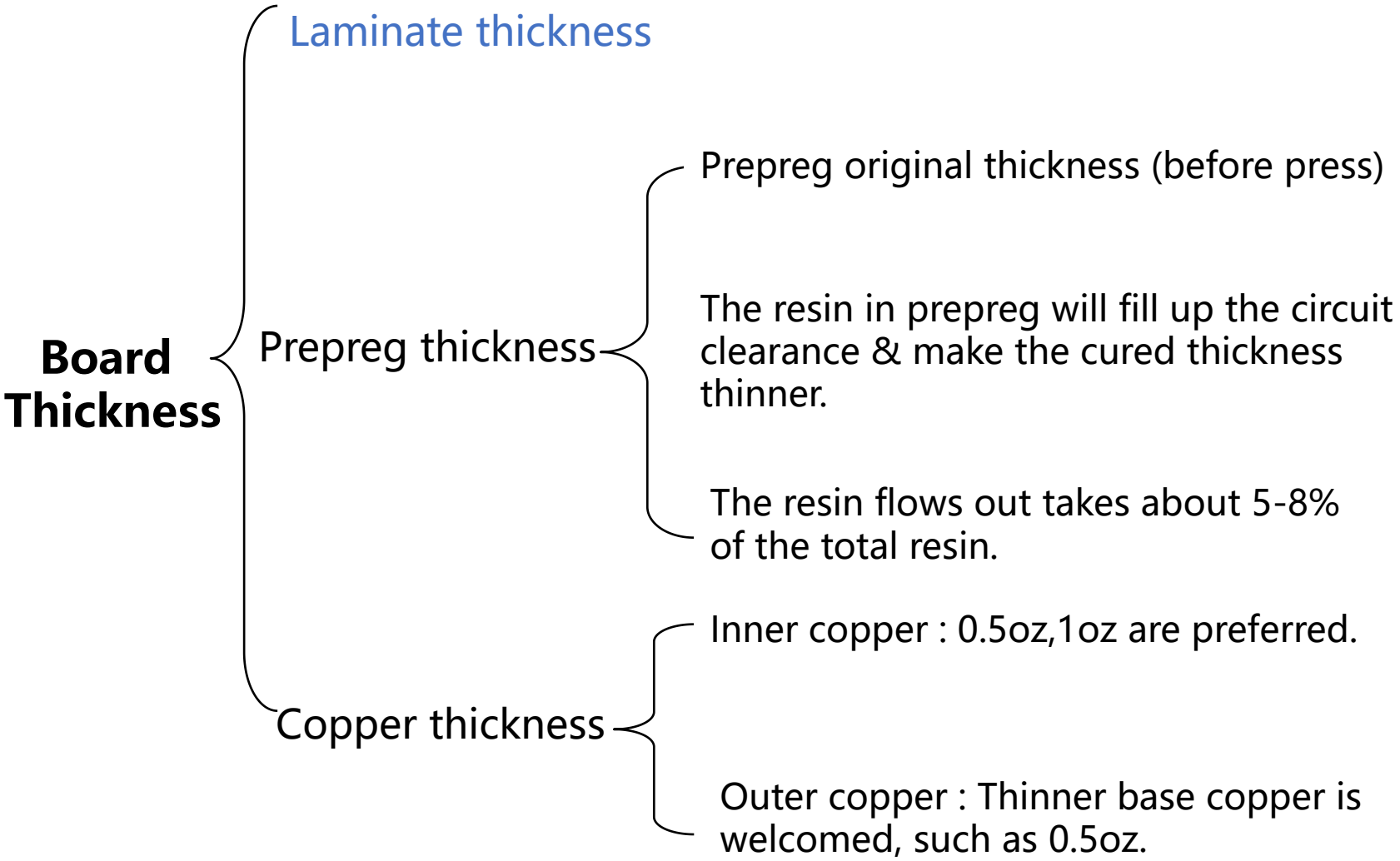
Laminate is in dielectric C-stage & covered by copper clad in both side.

It is used for inner layers & outer layer.

Prepreg is the bonding material in B-stage & to be used during the construction of multilayer boards, which is used to bond between layers.

Copper is pressured to be used as outer layers.




Board Thickness
Laminate thickness
Prepreg thickness
Prepreg original thickness (before press)
The resin in prepreg will fill up the circuit clearance & make the cured thickness thinner.
The resin flows out takes about 5-8% of the total resin.
Copper thickness
Inner copper : 0.5oz,1oz are preferred.
Outer copper : Thinner base copper is welcomed, such as 0.5oz.

PCB SAYFU

Below is the useful thickness of laminate, prepreg and copper.

Laminate	Tolerance
	IPC - 4101 Class B/L
4.0mil	+/-0.7mil
4.5 mil	+/- 0.7 mil
6.0 mil	+/- 1.0 mil
8.0mil	+/-1.5mil
10.0 mil	+/- 1.5 mil
14.0 mil	+/- 2.0 mil
16.0mil	+/- 2.0mil
18.0 mil	+/- 2.0 mil
24.0 mil	+/- 3.0 mil
28.0 mil	+/- 3.0 mil
40.0 mil	+/- 4.0 mil
47.0 mil	+/- 5.0 mil
59.0 mil	+/- 5.0 mil

Prepreg	Thickness before pressure
106	2.2 +/- 0.7mil
1080	2.8 +/- 0.7 mil
3313	3.7 +/- 0.7 mil
2116	4.5 +/- 0.7 mil
7628	7.9 +/- 1.5 mil

Copper type	Code	Thickness(μM)
1/3 oz	T	12.0 (0.47mil)
1/2 oz	H	17.1 (0.67mil)
1 oz	1	34.3 (1.35mil)
2 oz	2	68.6 (2.70mil)

Benefits :

[a] Material cost saving (20% more cost on using unbalanced copper clad or 2oz base copper)

[b] Better material supply (more flexibility on loading ramp up) (1-2 weeks longer in getting special material from market)

[c] Better inventory control (no need to store many kinds of materials for different projects)

Section B-2 : Material Type

Below is the common material type :

Type	Material Type	Supplier
Low-Middle Capability Produc	Normal Tg	SY S1141/ KB6150/ 6160
	Middle Tg FR4 (150°C)	SY S1000/ IT158 /KB6165
	HF FR4	SY S1155 (normal Tg) NanYa NPG-170(High Tg)
High Capability Product	High Tg FR4 (165°C min.)	S1000-2M, IT-180, KB6167
Speedy Data Transmit & High Thermal Capability Product	Low $D_{k\ reform}$ FR4	Getek ML 200 series
	Tg180 (BT Epoxy)	Polyclad GI180
RF / Microwave Use (High Frequency & Low Factor)	Non-polar organic resin + ceramic	Arlon 25FR series
	Glass-reinforced hydrocarbon/ceramic	Roger RO4350 series

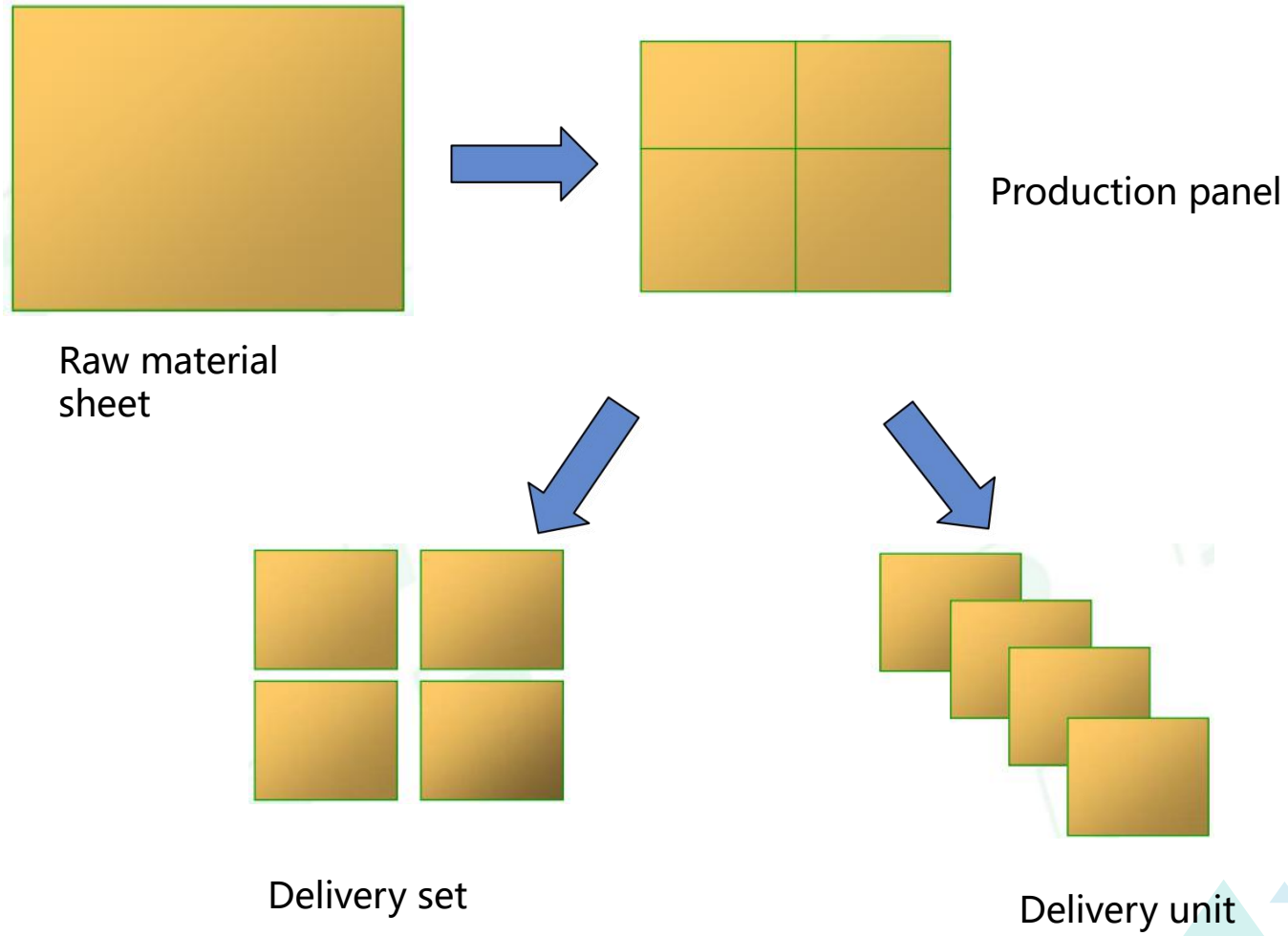
Remark :BT & Rogers are not commonly used, lead time is needed for reserve material.

Section B-3 : Production Panel Design

Production panel utilization directly determines raw material utilization and manufacturing efficiency. It relies on :

- Set size (delivery panel size) : the most important factor. Suitable set size will get the most efficient production panel size.
- Tooling area, which is used for fabricating the board together with the test coupon.

Panel Definition



For production panel design, there are some limitations to obey :

Standard Sheet Size :

- 36″ x 48″
- 42″ x 48″
- 18″ x 24″ (Rogers and other High Frequency material)

Section B-4 : Stack Up Design

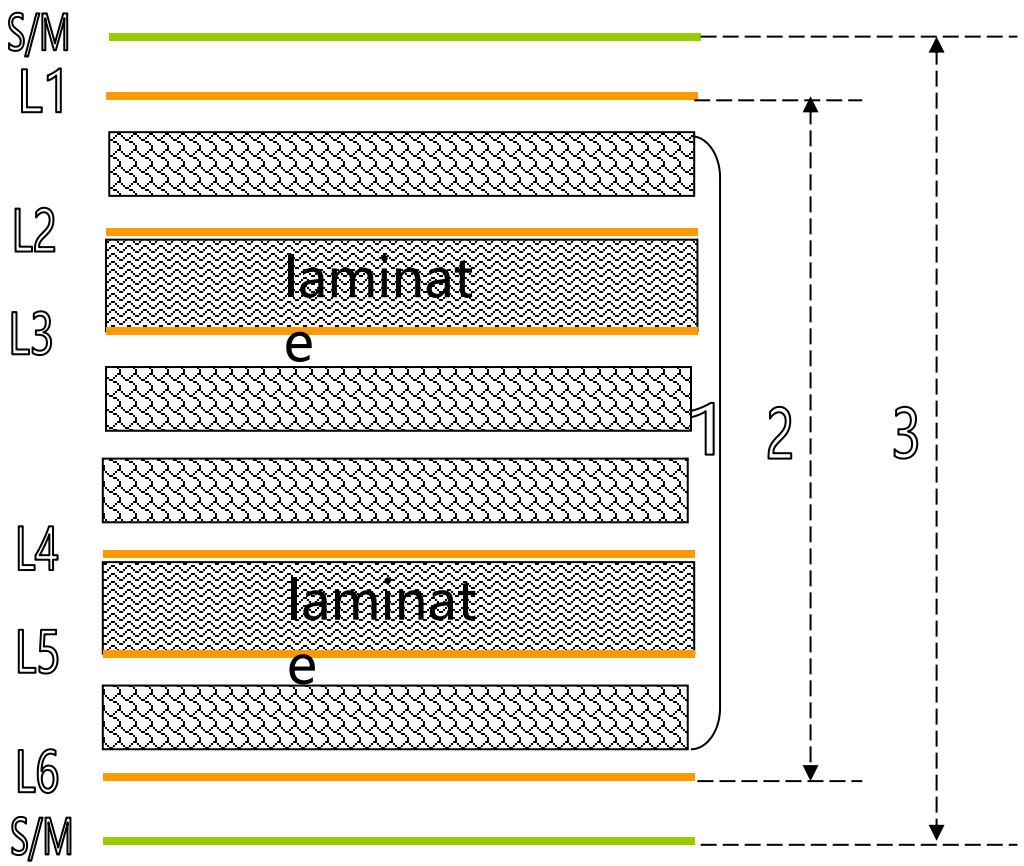
1. Stack up is preferred to be symmetrical. A symmetrical stack up is useful for controlling the expansion & shrinkage. The symmetrical will include :

- Material type should be uniform (no mixing of different Tg & material base).
- Dielectric thickness of layers.
- Prepreg glass type and ply number of layers.
- Copper thickness of layers and its distribution.
- Location of the signal layers and plane / power layers.

2. Definition of the board thickness requirement.

¢ Define the measurement of board thickness (see picture) : from solder mask to solder mask (3), or from copper to copper (2), or from laminate to laminate (1), or measure on the gold finger area etc. Highfive can select the suitable thickness to meet the right requirement.

¢ Specify the tolerance of board thickness. Generally speaking, if the overall thickness is more than 1mm, the tolerance should be +/- 10%; if less than 1mm, the tolerance should be +/- 0.1mm.



Propose …

- symmetric lay-up construction *(easy to control pressing*)
- common base material *(cost effective, shorter ordering lead time)*
- minimum number of prepreg *(cost saving, easy to control registration, avoid delamination)*

- unsymmetric lay-up construction *[e.g. 0.5oz+1080+7628+0.5oz)]*
- asymmetric base copper *[e.g. 0.5oz/1oz]*
- Hybrid material *[e.g. FR4 + Rogers or other non-FR4]*
- difficult to control bow/twist, shrinkage

Notes : Thickness is not the only indicator for material cost, other factors such as number of plies used, material type, thickness tolerance, & the demand for this material may affect the cost.

Effective Lay-up Design

4 Layers Construction (for normal thorugh via PCBs)

4 layer 0.5+/-0.1mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.10	+/-0.32		
	Prepreg (1080*2)	5.04	+/-0.4	3.8	0.019
L2	copper	0.63	+/-0.063		
	Core	6.00	+/-1.5	4.2	0.015
L3	copper	0.63	+/-0.063		
	Prepreg (1080*2)	5.04	+/-0.4	3.8	0.019
L4	1/2oz+plating	1.10	+/-0.32		
	Solder Mask	1.10	+/-0.86		

4 layer 1.6+/-0.16mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg (1080+2116)	6.94	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	44.50	+/-1.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg (1080+2116)	6.94	+/-0.4	3.8	0.019
L4	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		
	Total thickness				

Effective Lay-up Design

6 Layers Construction (for normal thorugh via PCBs)

6 layer 0.8+/-0.1mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg (106+1080)	4.56	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	5.00	+/-0.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg (1080+1080)	5.04	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	5.00	+/-0.5	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg (106+1080)	4.56	+/-0.4	3.8	0.019
L6	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

6 layer 1.6+/-0.16mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg (1080+7628)	10.07	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	14.17	+/-1.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg (1080+1080)	5.04	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	14.17	+/-1.5	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg (1080+7628)	10.07	+/-0.4	3.8	0.019
L6	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

Effective Lay-up Design

8 Layers Construction (for normal thorugh via PCBs)

8 layer 1.0+/-0.1mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg (1080+1080)	5.32	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	4.00	+/-0.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg (3313)	3.33	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	4.00	+/-0.5	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg (3313)	3.33	+/-0.4	3.8	0.019
L6	copper	1.40	+/-0.063		
	Core	4.00	+/-0.5	4.2	0.015
L7	copper	1.40	+/-0.063		
	Prepreg (1080+1080)	5.32	+/-0.4	3.8	0.019
L8	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

8 layer 1.6+/-0.16mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	11.81	+/-1.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg (2116)	4.05	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	9.84	+/-1	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg (2116)	4.05	+/-0.4	3.8	0.019
L6	copper	1.40	+/-0.063		
	Core	11.81	+/-1.5	4.2	0.015
L7	copper	1.40	+/-0.063		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L8	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

Effective Lay-up Design

10 Layers Construction (for normal thorugh via PCBs)

10 layer 1.6+/-0.16mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance(mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L6	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L7	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L8	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L9	copper	1.40	+/-0.063		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L10	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

10 layer 2.0+/-0.2mm

Layer	Mother Board	Typical layer thickness (mil)	Tolerance(mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	9.84	+/-1	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	9.84	+/-1	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L6	copper	1.40	+/-0.063		
	Core	9.84	+/-1	4.2	0.015
L7	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L8	copper	1.40	+/-0.063		
	Core	9.84	+/-1	4.2	0.015
L9	copper	1.40	+/-0.063		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L10	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

Effective Lay-up Design

12 Layers Construction (for normal thorugh via PCBs)

12 layer 1.6+/-0.16mm

Layer	Mother Board	Typical layer thickness	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	3.94	+/-0.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	3.94	+/-0.5	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L6	copper	1.40	+/-0.063		
	Core	3.94	+/-0.5	4.2	0.015
L7	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L8	copper	1.40	+/-0.063		
	Core	3.94	+/-0.5	4.2	0.015
L9	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L10	copper	1.40	+/-0.063		
	Core	3.94	+/-0.5	4.2	0.015
L11	copper	1.40	+/-0.063		
	Prepreg 2116	4.28	+/-0.4	3.8	0.019
L12	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

12 layer 2.0+/-0.2mm

Layer	Mother Board	Typical layer thickness	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/2oz+plating	1.40	+/-0.32		
	Prepreg 2116+1080	6.94	+/-0.4	3.8	0.019
L2	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L3	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L4	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L5	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L6	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L7	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L8	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L9	copper	1.40	+/-0.063		
	Prepreg 1080+1080	5.04	+/-0.4	3.8	0.019
L10	copper	1.40	+/-0.063		
	Core	5.90	+/-0.5	4.2	0.015
L11	copper	1.40	+/-0.063		
	Prepreg 2116+1080	6.94	+/-0.4	3.8	0.019
L12	1/2oz+plating	1.40	+/-0.32		
	Solder Mask	1.10	+/-0.86		

Effective Lay-up Design

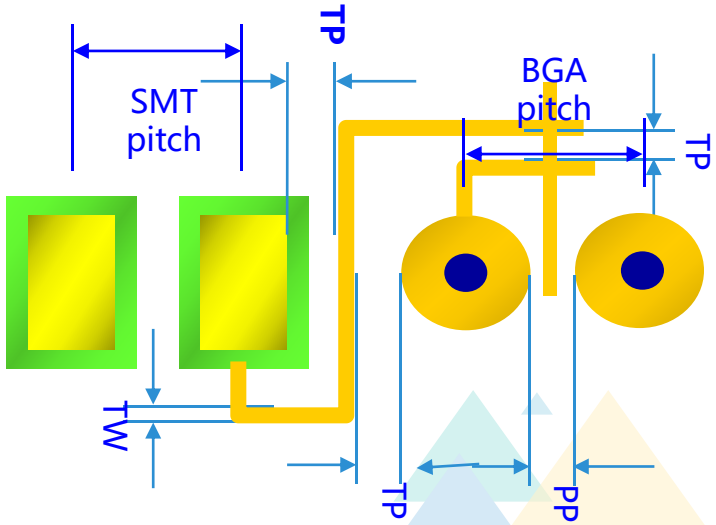
6 Layers Construction (for Microvia PCBs)
(Structure : 1+4+1, with blind and buried vias)

6 Layer 1.0+/-10%mm					
Layer	Mother Board	Typical layer thickness (mil)	Tolerance (mil)	Dielectric Constant	DF
	Solder Mask	1.10	+/-0.86		
L1	1/3oz+plating	0.94	+/-0.32		
	Prepreg (1080)	2.87	+/-0.4	3.8	0.019
L2	1/3oz+plating	1.10	+/-0.32		
	Prepreg (2116)	4.55	+/-0.6	4.1	0.017
L3	Copper	0.63	+/-0.063		
	Core	16.14	+/-2	4.25	0.015
L4	copper	0.63	+/-0.063		
	Prepreg (2116)	4.55	+/-0.6	4.10	0.017
L5	1/3oz+plating	1.10	+/-0.32		
	Prepreg (1080)	2.87	+/-0.4	3.80	0.019
L6	1/3oz+plating	0.94	+/-0.32		
	Solder Mask	1.10	+/-0.86		

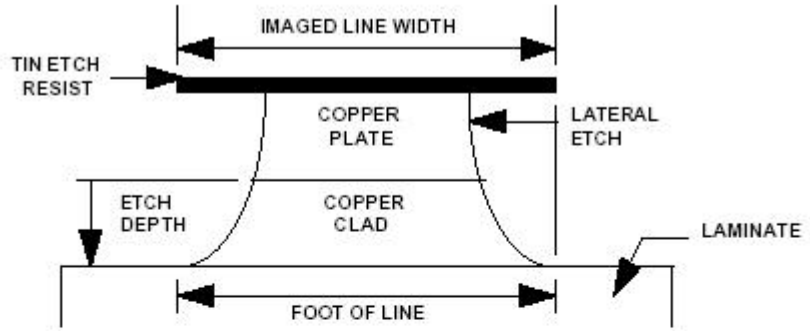
Section C : Circuit Design

Circuit Design includes Circuit Distribution, Circuit Density, Trace & Pad Design, Routing Trace, SMT/BGA Design. Below is some of the normal design :

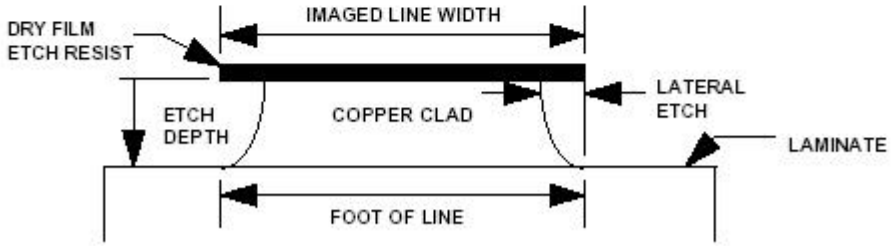
- Minimum trace width (TW) / spacing (TP) : 4mil / 4mil, 3mil/3mil partly
- Minimum annular ring width : 5mil for through hole, 4mil for vias
- Minimum spacing trace-pad (TP) and pad-pad (PP) : 4mil
- Minimum SMT pitch : 0.5mm, 0.4mm partly
- Minimum BGA pitch : 0.8mm, partly 0.5mm



Trace (pad) is reduced during the etching process, copper is etched in the laterally and bottom side, as shown below.



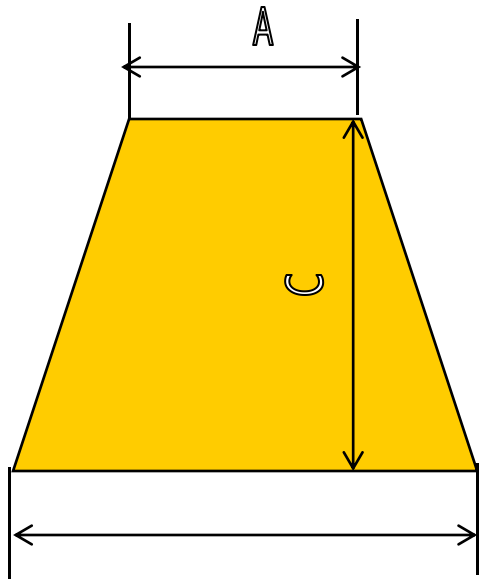
Outer Layer Line after Etching



Inner Layer Line after Etching

The etch part is mostly decided by etch copper thickness before image transfer : for inner layer it is the base copper, for outer layer it is the outer base copper + plated copper. The thinner the etch copper is, the easier the control of the line width and spacing.

0.5oz is preferred.



$$\textbf{Etch factor} = \frac{C}{(B-A)/2}$$

When etch factor is a constant value (controlled by >1.5 for inner layer, >3 for outer layer), the smaller the C is, the smaller (B-A)/2.

Gerber form

PCB Data	Drawing Data	Drill Data	Netlist drawing	Data Pack Form
RS274X (Gerber X)	RS274X (Gerber X)	Excellon II	IPC - 356-D	PkZip in DOS (.ZIP)
ODB++ (Genesis 2000)	Gerber Format	RS274X (Gerber X)	IPC - 356-A	WinRAR(.RAR)
Gerber with Aperture List	HPGL	Gerber Format		
Protel 99se / Altium Designer				
	AutoCAD (.dwg or .dxf) Version under 2004			
preferred				
RS274X (Gerber X)	RS274X (Gerber X)	Excellon II	IPC - 356-A	Self-extracting (.EXE)
ODB++	HPGL			PkZip in DOS (.ZIP)

Suggestion :
1. Recommend to describe in Chinese or English.
2. Give the netlist file so as to check the circuit open or short.
3. Do not give the useless file for PCB fabrication, such as assemble drawing.

Section C-1 : Circuit Distribution and Density

For outer and inner layer, the circuit distribution and density is preferred to be symmetrical and uniform. Therefore, adding thieves for outer layer and inner layer is more workable for pcb fabrication.

Benefits to Customer :

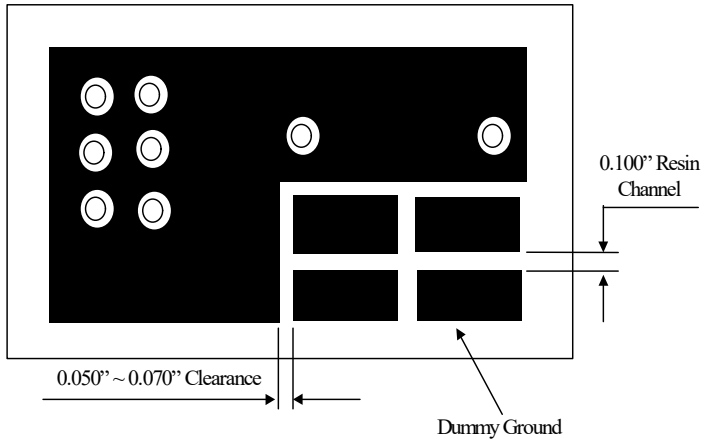
- Rigidity for assembly process.
- Promote adhesion with solder mask (SM) as Cu/SM adhesion is better than dielectric/SM.
- Improve resistance against fiducial damage (scratch, pit plating).

Benefits to Manufacturer :

- Standardize copper area (current density) for all projects (plating time is fixed).
- Improve control of outer layer etching due to consistent copper density.
- Improve control of pressing due to "regulation" of coaxial flow of resin of high temp / high pressure treatment.
- Resistance to warpage during thermal process (S/M curing, baking, etc.).

suggest to add the thieves, below are some normal format :

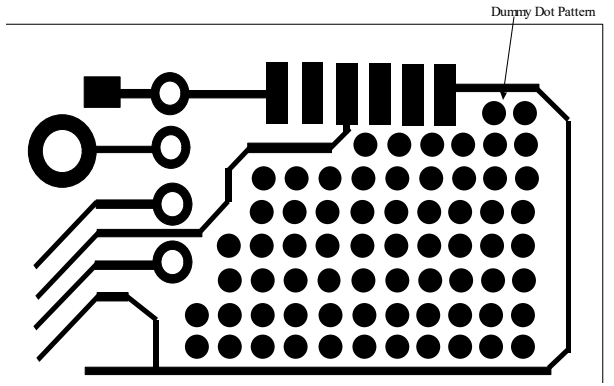
1) Dummy Copper Ground on inner layer :
Full ground with 100 mil resin channel for every 2" of length. Keep 50 mil clearance away from holes, slots and other circuitry.



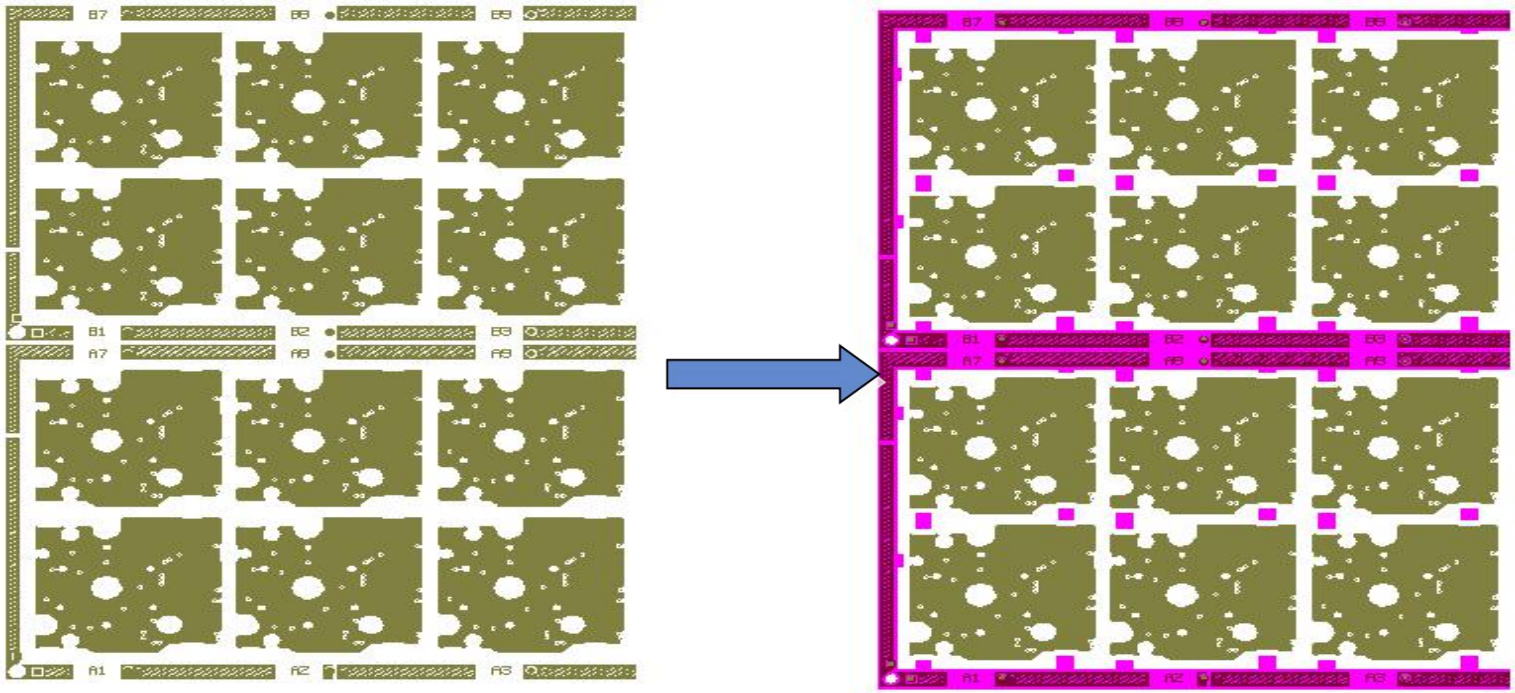
2) Dummy Pattern on spacious area :

- 75 mil copper dot in pitch of 150 mil.
- 75 mil copper diamond in pitch of 150 mil.

* *Keep 50-70 mil clearance away from holes, slots and other circuitry*



Dummy Copper Ground / Net on outer layer in the breakaway tabs should be covered with solder mask to save ENIG cost :



Free of solder mask

Pink area stands for solder mask

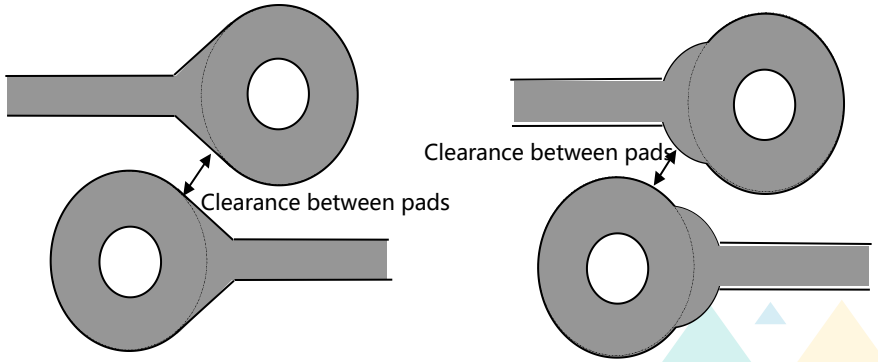
Not Recommended → Add the solder mask → Recommended (Solder mask cover the dummy copper ground or Net ⇒ Save the gold cost).

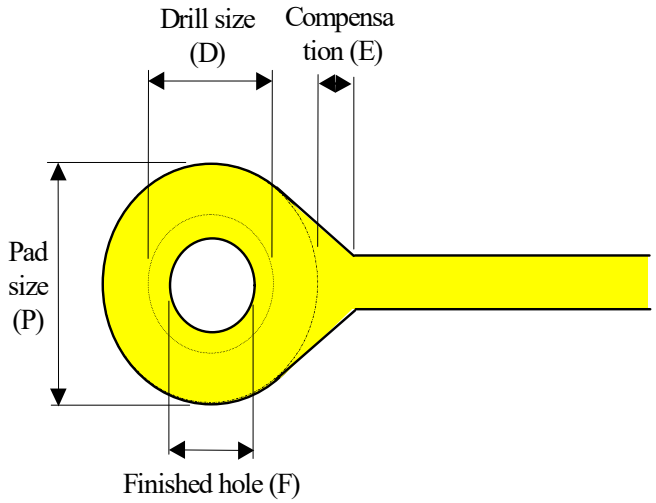
Section C-2 : Tear Drop Design

For the connection between pad and line, Highfive suggests the tear drop design :

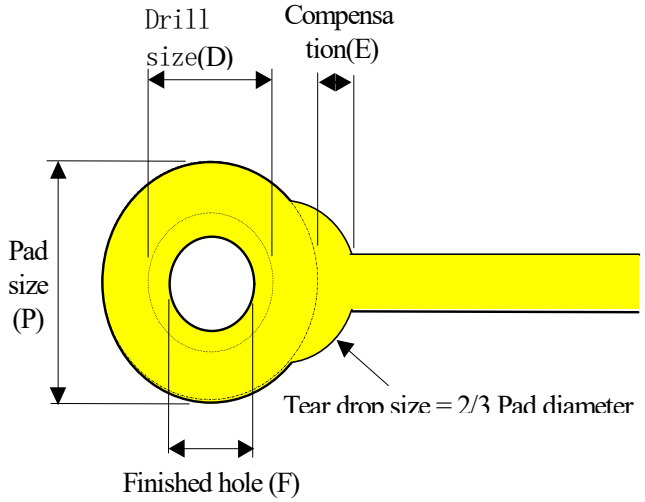
- Ensure there are enough annular ring for plated hole.
- The connection can be protected better by solder mask, for the combination between solder mask and copper is better than that of laminate.
- More space for the registration of drill hole.

We prefer the tear drop to be in the form of triangle, because it can control the clearance between pads.





Triangle form



Snow man form

A. Define

Annular ring = (P - F)/2 + E

C.experience Value

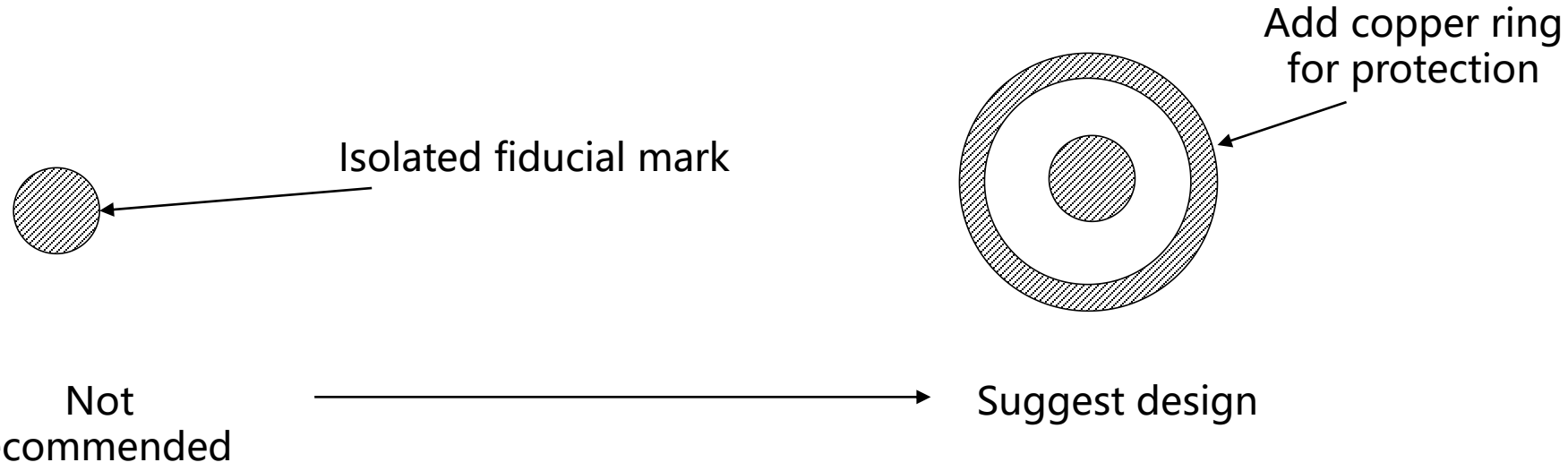
Compensation (E) = 2 - 3 mil

Drill size (D) = F + 2 mil

B. Tear drop design

Min.finished A/R	Tear Drop add
3 mil	P - F < 16
2 mil	P - F < 14
1 mil	P - F < 12

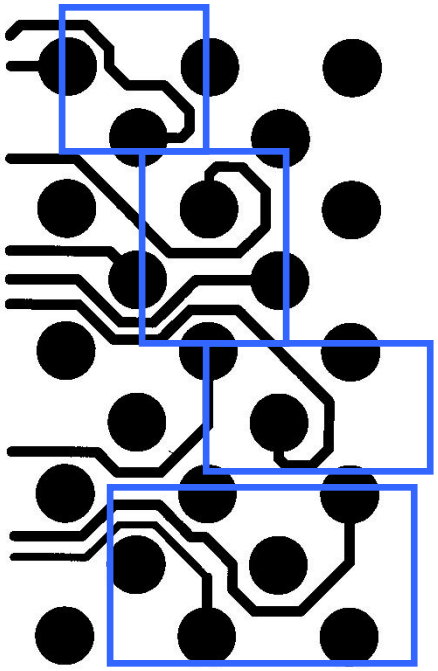
Section C-3 : Fiducial Mark Design



For the design of isolated fiducial mark, it may be peeled off in the manufacturing process. Adding a copper ring can protect it from peeling off.

Section C-4 : BGA and SMT Design

Prevent unfavorable design at BGA



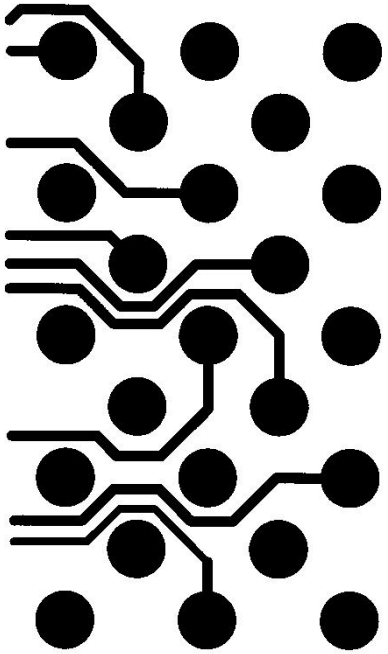
High density of drilling and traces

🡐 Unfavorable design, not recommended.

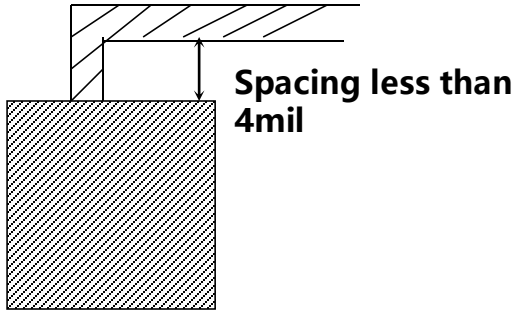
- easy to cause open by film residues.
- extended trace pass more grids, increase trace within grid, reduce line to pad/line spacing.

More simple design 🡒

- greater operation window.
- reduce open/short problem.
- more chance to use larger drill bit, more efficiency on drilling.



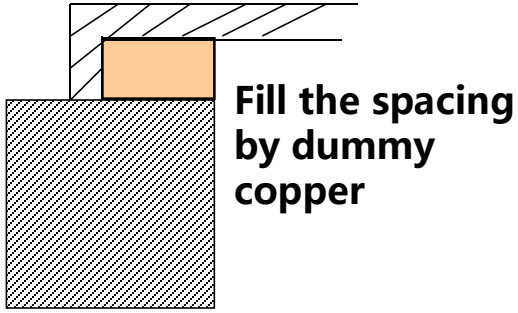
Prevent unfavorable design near SMT Pad

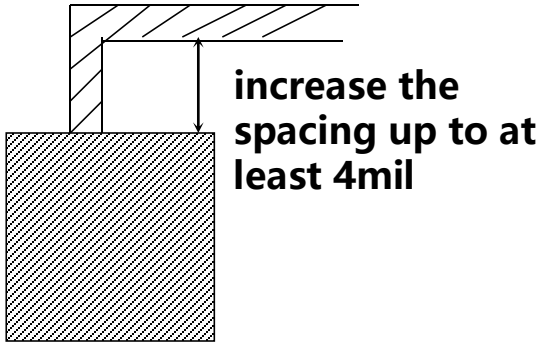


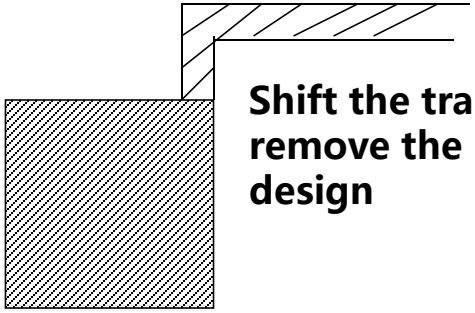
Unfavorable design, not recommended :

- easy to cause circuit open by film residue.

Suggestions (suitable for production) :





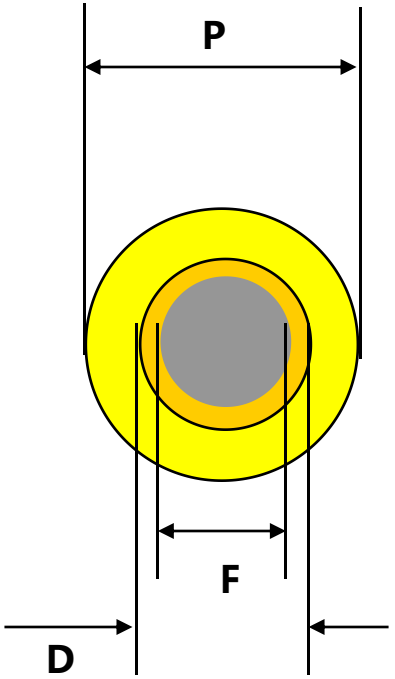


✓ It is strongly recommended to apply above design in the project.

Section D : Hole Design

Finished hole (F) is affected by the following factors :

- Drill size : D
- Landing pad size : P
- Hole tolerance
- Copper thickness on hole wall

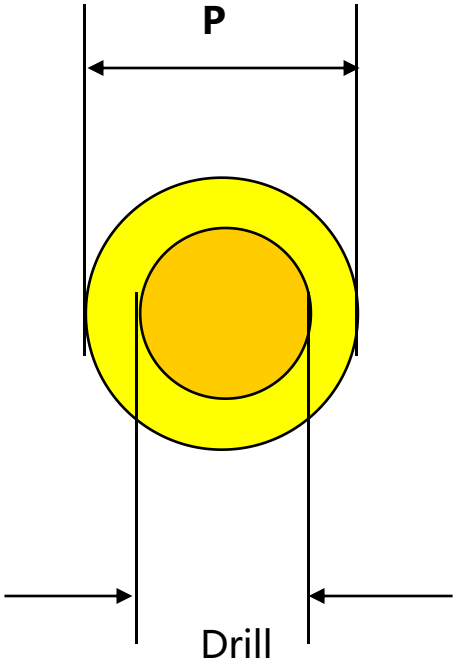


Section D-1 : Annular Ring Design

Annular Ring :

Finished annular ring = (P - F) / 2 - A

P - pad size, F - finished hole
A - image transfer, layer registration and drill tolerance



Notes :

- Usually "A" is 5 mil for through hole, 4 mil for blind-via.
- To adjust the pad size to ensure enough annular ring.
- Prefers drill size 0.25mm as the minimum size.

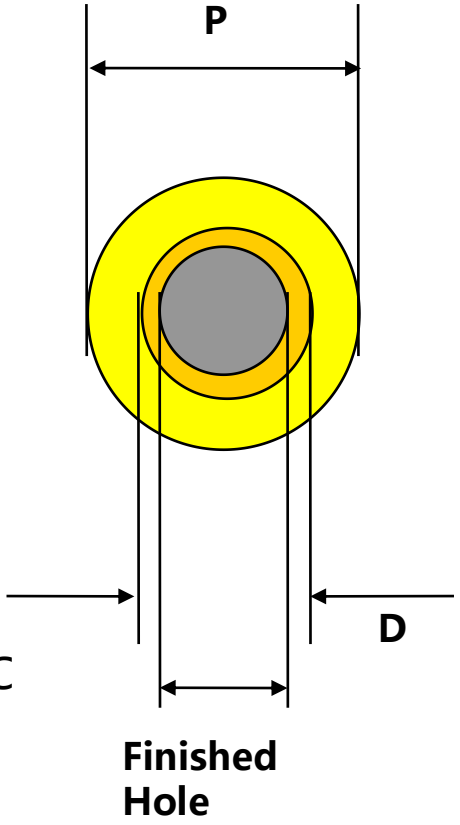
The cost for drill size 0.2mmwill be higher.

0.15mm drill size is only for PCB thickness less than 0.6mm

HWTC (Hole Wall to Conductor) Calculation :

Formula : HWTC = (P - D) / 2

P - Clearance pad size at inner layer
D - Drill bit size



Remark :

- HWTC is critical factor on controlling inner short (caused by drilling)
- customer can adjust the clearance pad size to obtain sufficient HWTC
- the capability on minimum HWTC is 8mil
- clearance between drilled hole to inner layer ground (HWTC) is 8 mil.
  Min. spacing between two holes is at least 12 mil.

Section D-2 : Drill Size & Tolerance

- The number of hits, stack height, minimum drill size and the types of holes are the critical factors of drilling. Selection of minimum drill size is very important on the cost.
- Minimum drill size is selected according to the customer requirements, such as finished hole, annular ring, hole tolerance, board surface treatment & copper thickness on wall.
- Normally, base on 5mil annular ring and positive/minus hole tolerance, for HASL surface, drill size = finished hole + 6 mil

  for other surface, drill size = finished hole + 4 mil

Minimum drill size is 8 mil (0.2mm)

Maximal drill size is 236.22 mil (6.0mm)

Drill size is in 0.05mm increment, besides, there are some special size 0.711mm(pressfit), 3.175mm for strict hole tolerance

Hole\Tolerance	Plated	Mass production		Capability	
		Length	Width	Length	Width
Hole	Yes	+/- 3mil		+/- 2mil for sample	
	No	+/- 2mil			
overlap-drill slot	Yes	+/- 5mil	+/- 4mil	+/- 5mil	+/- 4mil
	No	+/- 5mil	+/- 4mil	+/- 5mil	+/- 4mil
Hole registration +/- 3mil, re-drill registration +/- 6mil					

Note : *The overlap-drill slot width should not be less than 0.8mm. And plated overlap-drill length is preferred not longer than 6mm due the reduction of efficiency.*

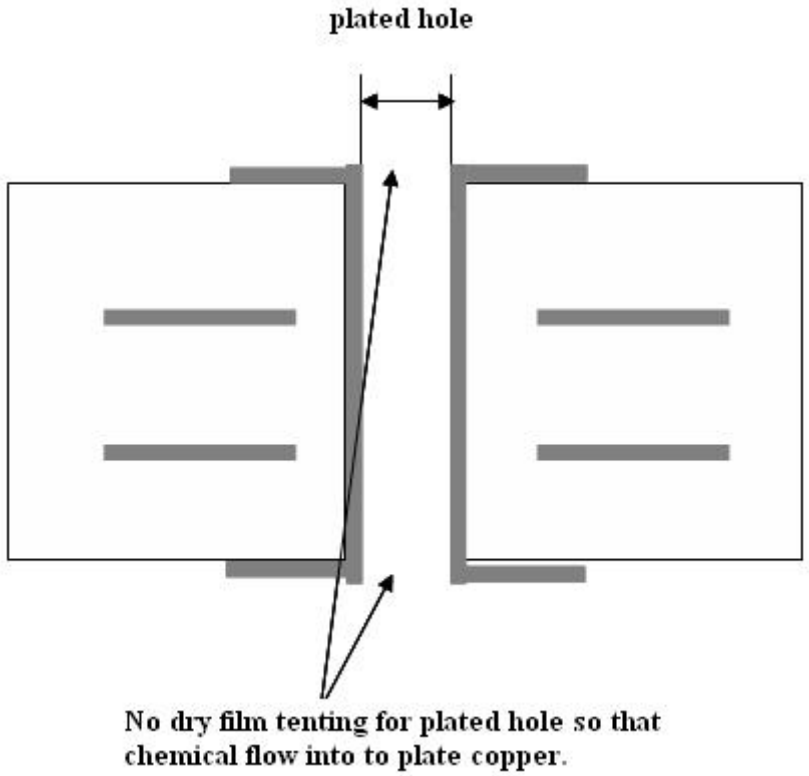
Section D-3 : Hole Design

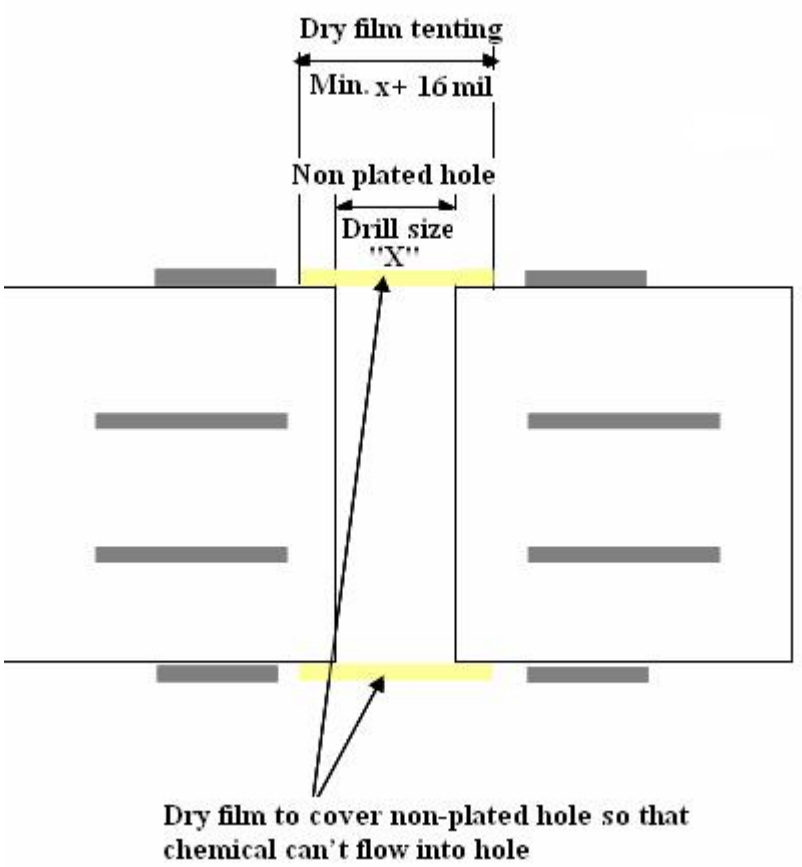
In the process of image transfer, dry film will cover those non-plated hole and get opening for plated hole (refer to the next page).

¢ Plated hole (include through hole and buried-via) should have pad in outer layers, otherwise, it will affect the quality of copper plated.

¢ Non-plated hole should have 8 mil copper clearance from hole edge for dry film tenting. If there is not enough clearance or no clearance for dry film tenting, re-drill (2nd drill) process will be added & the registration is +/- 6mil.

It is not recommended → no pad in outer layer for plated through hole (buried-via); design pad in outer layer for non-plated hole.


plated hole
No dry film tenting for plated hole so that chemical flow into to plate copper.


Dry film tenting
Min. x+ 16 mil
Non plated hole
Drill size "X"
Dry film to cover non-plated hole so that chemical can't flow into hole

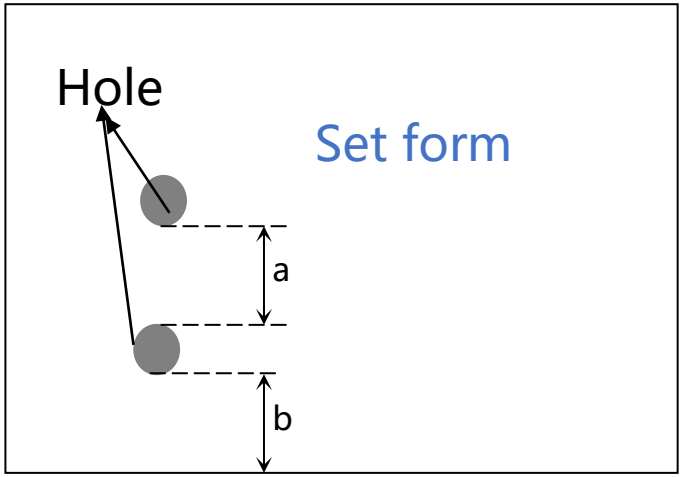
Some holes are close to other holes or outline, it is easily to get breakout. Refer to picture in right:

¢ a>12 mil:

The spacing should be minimum 12 mil from hole edge to edge.

¢ b>15 mil:

The spacing should be minimum 15 mil from hole edge to outline.



Aspect Ratio (for plating)

AR = T : D

¢ Through hole

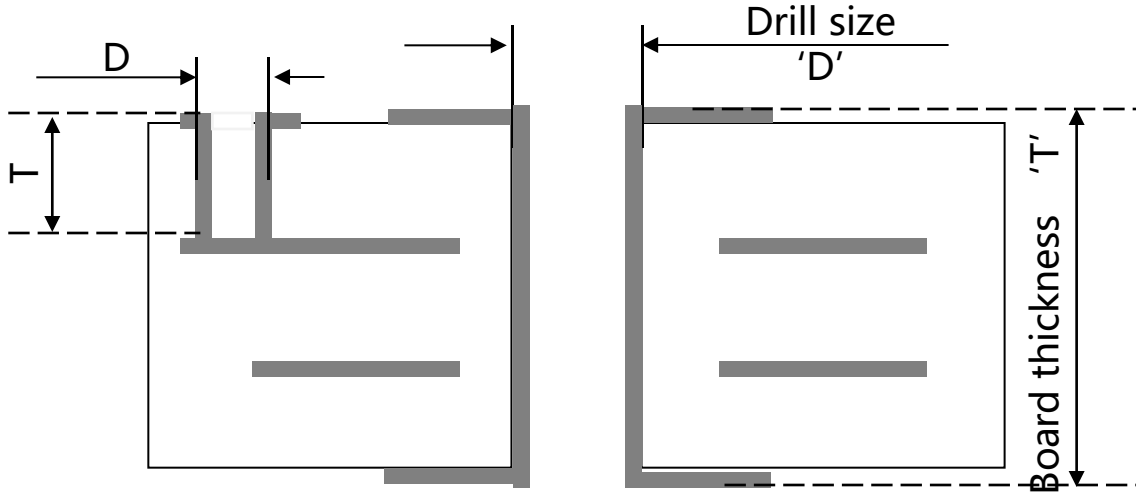
AR <= 8:1 is preferred.

AR <= 12:1 is our max capability.

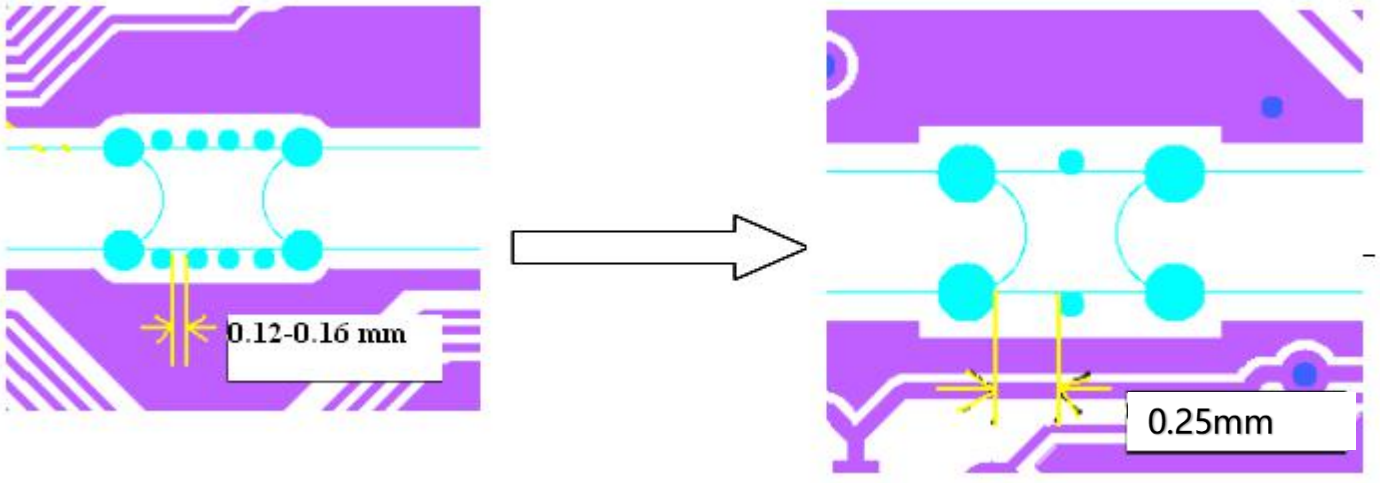
¢ Blind-via

AR <= 0.6:1 is preferred.

AR <= 0.75:1 is our max capability.



Recommendation on design of breakaway tab (hole spacing) :



Not Recommended → increase efficiency → Recommended (fewer holes, wider non-drill spacing ⇒ not easy to break when assembly)

Section E : Solder Mask

Available solder mask color are green, matt green, blue, black, white and red， yellow.

Colour	Type	Supplier	Remark
Green	H-9100 3G	Rongda	
	KSM-6188/6189	KUANGCHUN	
	LP-4G/G-05	NANYA	
ALL	H-8100	Rongda	
	YSR - 900	YEYO	
White	PSR-4000 WT02	Taiyo	
		Taiyo	

Below are the limitation in the solder mask process :

¢ Solder mask registration : +/- 2 mil is our min., +/-3 mil is preferred.

¢ Solder mask thickness on trace : 0.5 mil~1 mil

¢ Solder mask clearance : minimum 3 mil

¢ Solder mask line cover: minimum 3 mil

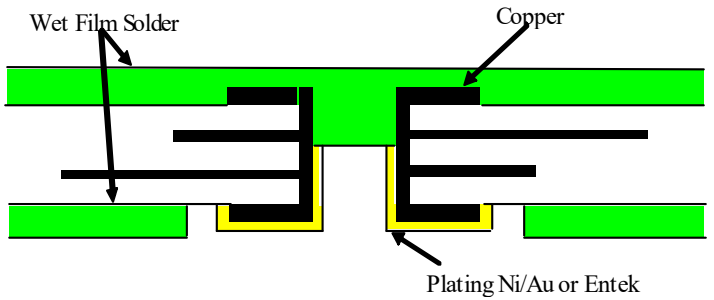
¢ Solder mask dam : minimum 4 mil for green solder mask only, others need be 5mil at least.

¢ SMT/SMD/BGA pad spacing (require solder mask dam) : 8 mil is preferred for 1oz final copper

Section E-1 : Tented Via (Via Plugging)

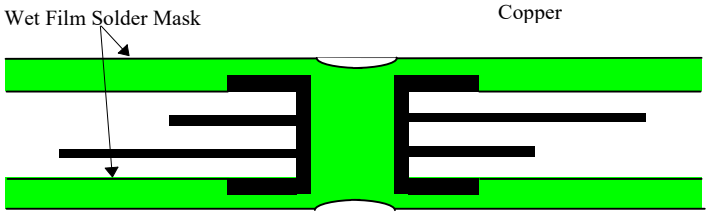
¢ *Single Side Tented Via*

- Suitable for Entek and plating Ni/Au;
- Not suitable for Hot Air Solder Leveling (HASL) and Immersion Au/Silver/Tin which may cause solder balls and chemical trapped inside the hole.
- For board thickness below 1mm, we suggest to add the solder mask opening for tented side to prevent solder mask plug into the via holes.



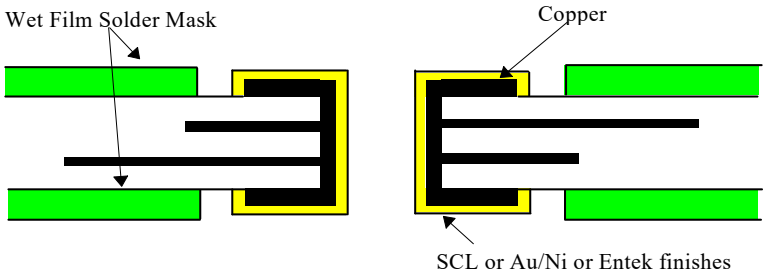
¢ Double Side Tented Via

- Suitable for all kinds of finishes
- Wet on wet printing, aluminum stencil-plugging & low-temp curing.
- Hole size less than 0.5mm.



¢ *Open Via*

no plugged for open vias in both side, the min. vias size need be 0.5mm to avoid tin balls inside of vias.



Section E-2 : Partially Via Plugging

Via with solder mask plugging partially

- Bleeding ink on the unexposed area after thermal curing
- Solderable surface contamination
- Poor appearance
- High scrap rate
- Much effort on reworking

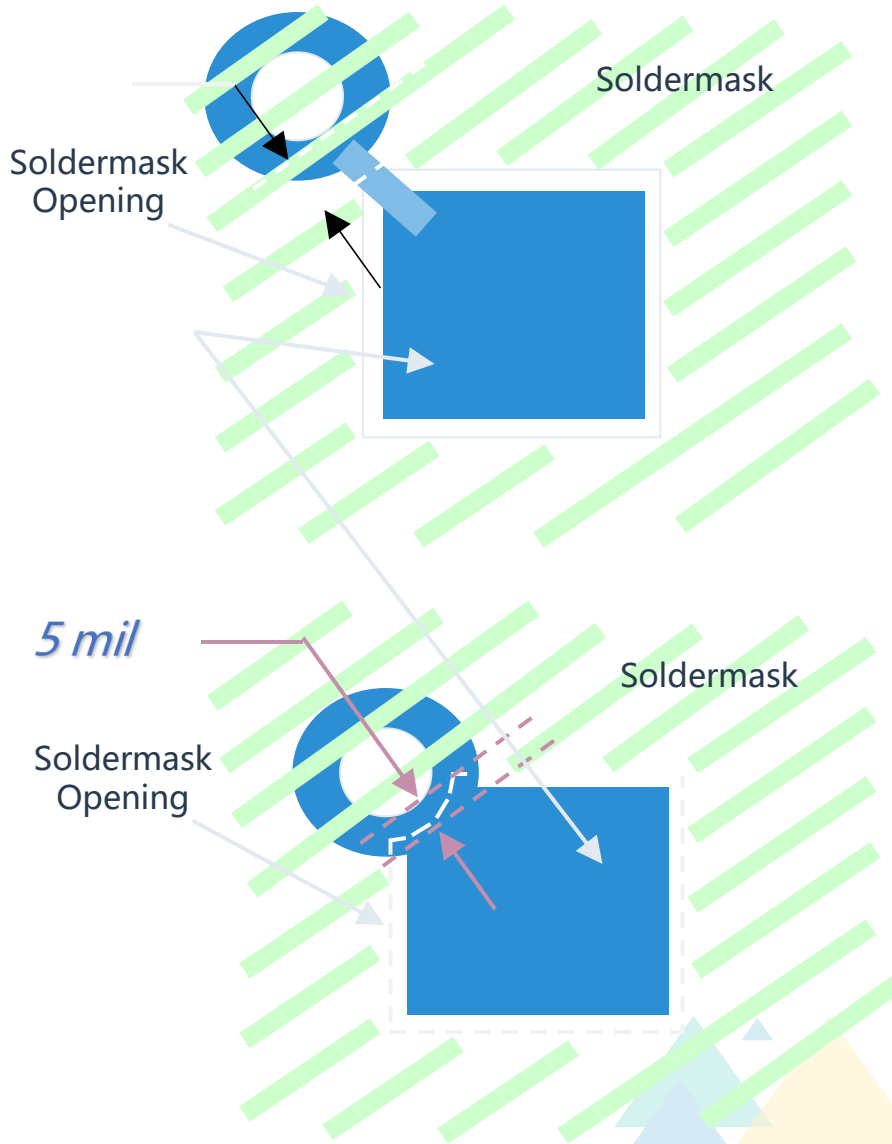
Via with soldermask plugging completely

Option I (Preferred)

- Move the via away from SMT to make it completely plugging
- Keep 5 mil min. distance between drilled via and soldermask opening

Option II

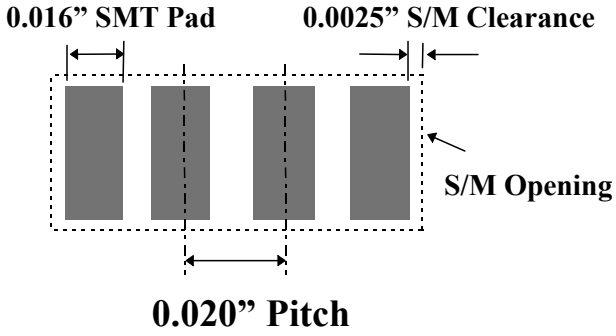
- Trim the soldermask opening to keep 5 mil min. soldermask coverage from edge of drilled via.
- Effective solderable area will be reduced



Section E-3 : Gang Relief on Fine Pitch

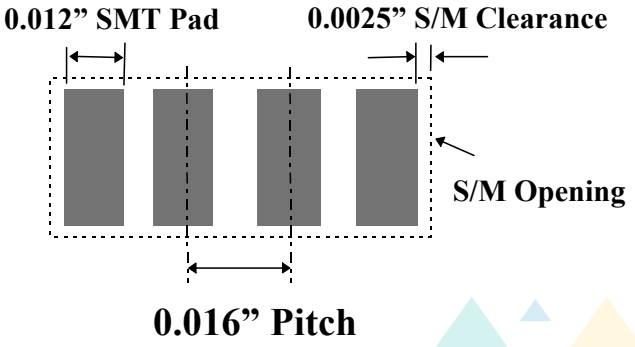
0.020" SMT Pitch

Max. SMT pad width : 0.016"
Min. S/M Clearance : 0.0025"
S/M opening : Gang relief
(Remove S/M bridge)



0.016" SMT Pitch

Max. SMT pad width : 0.012"
Min. S/M Clearance : 0.0025"
S/M opening : Gang relief
(Remove S/M bridge)



Section F : Outline Design

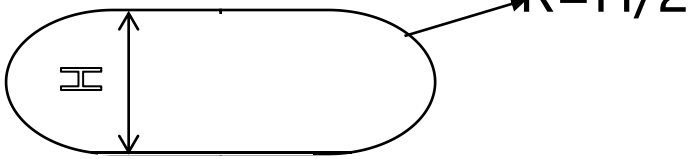
Section F-1 : General Outline Profiling

- Application of inside corner of R 0.047" max, R 0.016" min.
- Adding outside corner R 0.050" +/- 0.010" on the board to prevent scratching between board in handling.
- Applying V-cutting angle of 20°,30°, 45°with +/- 5° tolerance, prefer 30°
- Applying three NPT hole as datum for outline profiling.
- Applying some NPT hole for electrical test guiding.

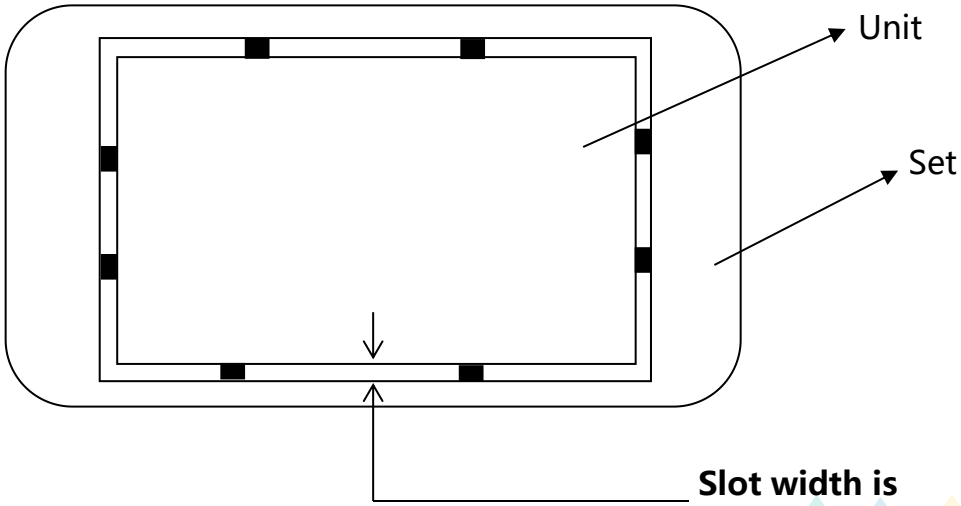
- *Tolerance*
  - Hole to hole +/- 0.004”
  - Hole to edge +/- 0.005”
  - Edge to edge +/- 0.005”
  - Datum to V-groove +/- 0.005”
  - Top & bottom V-groove +/- 0.003”
  - V-groove web thickness +/- 0.004”
  - Beveling depth +/- 0.004”
  - Routing +/-0.005’ ’

Section F-2 : Slot Design

- Plated slot is recommended to be full radii form, the width is less than 0.6mm.
- Non-plated slot tolerance is minimum +/- 5 mil for both width and length.
- Separate slot width (see below right picture) is suggested to be not less than 1.2mm due to the low efficiency, 2.0mm or 2.4mm is welcome.



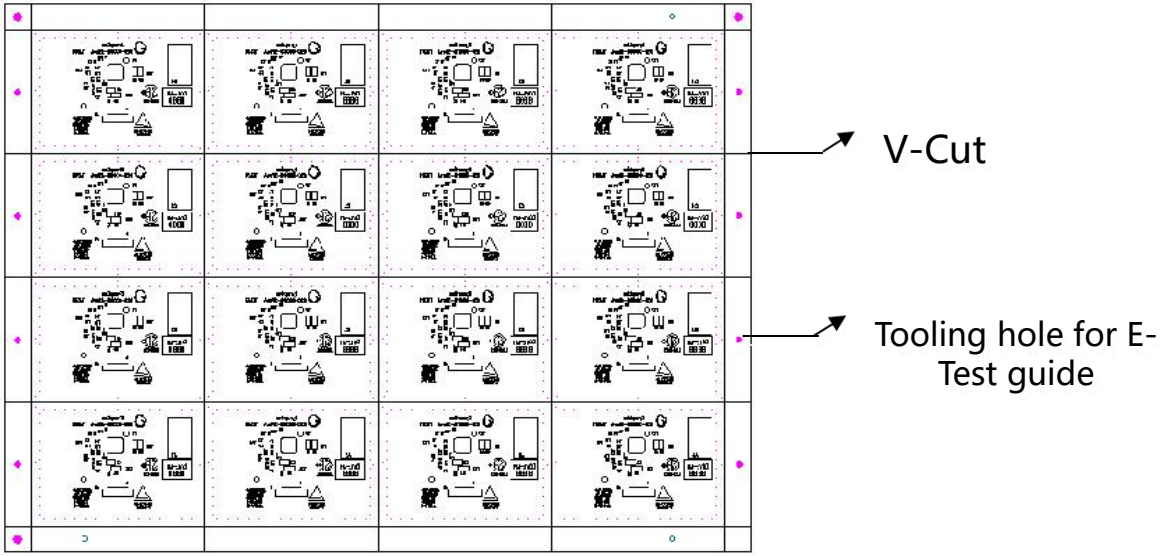
Full radii form slot



Section F-3 : For Halogen Free Material HighTg / PTFE Material Design

Due to the characteristic for halogen free material and High Tg material, it is not easy to apply punching, so we suggest to change the design from punch to V-Cut if possible.

For High Frequency material such as PTFE materia(AD1000, RT5800 etc.), panel form should be avoided, single PCB is fine. Otherwise there will have too much burrs and material is crisp, it is easy to break during process.



Section G : Surface Treatment

The available surface treatment is HASL, OSP, Immersion Tin, Immersion Silver, Immersion Gold, OSP+ENIG, Plating Gold.

Item\Surface Treatment	OSP	HASL	Immersion Tin	Immersion Silver	Immersion Gold	OSP + Immersion Gold	Plating Gold
Thickness (um)	02~0.6	1~40	tin≥1.0	0.2~0.4	Ni : 3~5 Au : 0.05~0.1	Ni : 3~5 Au : 0.05~0.1 Entek : 0.2-06	Ni : 3~5 Au : 0.025min
Cost	1	2	3	4	5	6	7

Note : 1 = cheaper ⟶ 7 = expensive

Thanks